



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,166	03/04/2002	Afshin Momtaz	019717-003100US	9226
20350	7590	09/27/2005	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP			WONG, LINDA	
TWO EMBARCADERO CENTER			ART UNIT	
EIGHTH FLOOR			PAPER NUMBER	
SAN FRANCISCO, CA 94111-3834			2634	

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/092,166

Applicant(s)

MOMTAZ ET AL.

Examiner

Linda Wong

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20 and 21 is/are allowed.
- 6) ☒ Claim(s) 1 and 15 is/are rejected.
- 7) ☒ Claim(s) 2-14 and 16-19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. **Claims 1 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Pasqualini (US Patent No.: 6397374), further in view of Schuur (US Patent No.: 5590157) and further in view of Peragine (US Patent No.: 6623185).
  - a. **Claim 1**, Whitt discloses a signal timing circuit comprising a clock recovery circuit (Fig. 2, label 2), a flip-flop coupled to receiving the recovered clock signal (Fig. 1, labels clock signal and 20) and an input signal (Fig. 1, label 10), an integrator coupled to the output of the flip-flop (Fig. 1, label 35), a comparator receiving an output from the integrator (Fig. 1, labels Vvar and 50) and a threshold (Fig. 1, label Vref). Although Whitt fails to show a switch for resetting the integrator, Schuur discloses an integrator comprising a switch for resetting. (Fig. 3A, label 8) Although Whitt does not teach a delay circuit, Pasqualini discloses a delayed data connected to a flip-flop. (Fig. 3, labels 310 and 110) It would be obvious to one skilled in the art to delay the data input to prevent hold time violation for the flip-flop. (Col. 2, lines 66-67 and Col. 3, lines 1-10) Although Whitt, Schuur, and Pasqualini fail to teach a delay circuit configured to

shift the phase in a manner symmetrical with respect to a sampling edge of the clock signal, it would be obvious to one skilled in the art to perform such a task to avoid error before and after the sampled edge. Although Whitt, Schuur and Pasqualini does not explicitly disclose a loss of signal detecting system, Peragine discloses a clock recovery circuit and a loss of signal detector. It would be obvious to one skilled in the art to art to incorporate the details disclosed by Whitt, Pasqualini and Schuur in the invention of Peragine to measure the performance of a communication level by detecting a loss of signal accurately and consistently.

- b. **Claim 15** inherits the limitations of a flip-flop and single delay circuit recited in claim 1 but claim 1 does not recite all the limitations of claim 15. Peragine discloses a loss of signal detector comprising a clock data recovery circuit for receiving an input signal and outputting a recovered clock (Fig. 2, labels Data and 32.77MHZ Clock), a retiming circuit for receiving the input signal and outputting a retimed data (Fig. 2, labels Data and Retimed Data) and a loss of signal detector for receiving an input signal, a recovered clock signal (Fig. 4, labels 426 and 424 and output from label 402). It would be obvious to one skilled in the art to art to incorporate the details disclosed by Whitt, Pasqualini and Schuur in the invention of Peragine to measure the performance of a communication level by detecting a loss of signal accurately and consistently.

***Allowable Subject Matter***

2. **Claims 2-14, 16-19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
3. **Claims 20 and 21** are allowed over prior art due to the recited limitation "latching the recovered clock signal using the delayed data signal as clock to generate an error signal, wherein a signal latch generates the error signal whenever a transition of the delayed data signal falls outside of the range  $(T/2) \pm \Delta T$ , where T is the period of the recovered clock signal".


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong

  
**STEPHEN CHIN**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2600**